ARL-BAA - W911NF-07-1-0498
Under topic: 2.16 RF Devices and Integrated Circuit Technology

Sb-Based Double Heterojunction Bipolar Transistors (DHBTs) with Fmax > 650GHz for 340GHz Transmitter

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UIUC SWIFT Final Progress Report

Table of Contents:

Statement of the problem studied:

In the Seeding 2 phase of SWIFT, UIUC was to complete 3 tasks: **(a)** develop and demonstrate a type-II DHBT with an f_T/f_{MAX} greater than 400/650 GHz with a breakdown voltage of greater than 5V, **(b)** develop a large signal DHBT model to model this newly fabricated device and enable the design of a power amplifier, and **(c)** design and simulate a 340 GHz power amplifier with this newly developed type-II model.

UIUC successfully fabricated a world record type-II device with f_T/f_{MAX} of 690/185 GHz having a breakdown voltage of 3.2V (W. Snodgrass, et al. IEDM 2007), and a device for which f_T was traded off for increased f_{MAX} of 480/420 GHz (f_T/f_{MAX}) with an increased breakdown voltage of 4.3V. UIUC has a clear plan for the development of a 400/650 GHz device that will involve the use of material from a commercial vendor and new fabrication techniques. Updates were made to UIUC's type-I SDD2 model, which has been proven to be superior to the industry standard VBIC model in modeling type-I DHBT operation, to model type-II device operation. This type-II SDD2 model was then used to model the fabricated 480/420 GHz device. Parameters of this model were shifted to approximately reflect the new material and fabrication techniques, which resulted in a modeled 480/600 GHz device. This projected model is then used to design a 340 GHz MMIC power amplifier with a gain greater than 10 dB and an output power of more than 10 mW.

Timeline:	***Tasks***
Seeding 2 **(4/07 to 3/08)**	• ***Task S2(a): Demonstrate Type II Sb- DHBT with f_{MAX} > 650 GHz, f_T > 400GHz & BVceo> 5V*** • ***Task S2(b): Develop large signal DHBT model (SDD2-POWER) to enable power amplifier design.*** • ***Task S2(c): Design/Simulation 340 GHz MMIC power amplifier with gain > 10 dB and Pout > 10 mW***

Figure O-1: UIUC statement of work for the Seeding 2 phase of SWIFT

Summary of the most important results:

Task S2(a): Demonstrate Type II Sb-DHBT with $f_{MAX} > 650$ GHz, $f_T > 400$ GHz & $BV_{ceo} > 5V$

Pseudomorphic heterojunction bipolar transistors (PHBTs) based on collector and base grading of the type-I InP/InGaAs SHBT material system have achieved record current gain cutoff frequencies in excess of 700 GHz. Type–I double heterojunctions transisitors (DHBTs) based on the same material system have sought to provide speeds competitive to those of the SHBT while maintaining higher breakdown voltages and better thermal characteristics due to the larger energy gap and more thermally conductive InP collector. However, the complicated grading schemes required to eliminate the current blocking conduction band discontinuity at the base/collector junction of the type-I DHBT undermines these advantages as the structures are vertically scaled to the dimensions required to achieve state-of-the-art f_T values. The grading schemes required for type I DHBTs often implement InGaAs spacers or quaternary grading layers; such transition layers are typically 40 to 60 nm thick, and present a fundamental limit to vertically scaling the device using collector thicknesses less than 70nm.

The type-II InP/GaAsSb HBT material system is a much more favorable alternative to both the InP/InGaAs SHBT and DHBT because of the higher breakdown voltages and better thermal conductivity achievable with the all InP collector. In addition, the positive conduction band offset of the base-collector heterojunction not only eliminates the conduction band discontinuity that plagues type-I DHBTs, but rather, provides an additional transit time reduction due to electrons being launched into the collector with initial kinetic energy due to the staggered conduction band lineup. These advantages have led to rapid progress in increasing device bandwidths, allowing competitive RF performance with established SHBT and type-I DHBT technologies.

Figure A-I details cutoff frequencies versus breakdown voltages for various device topologies and material systems, and illustrates that the scaling of InP/GaAsSb DHBTs is on track to provide breakdowns of 3 V at cutoff frequencies of 1 THz. By observing the trends for each system, it becomes apparent that the only systems capable of achieving THz bandwidths *while maintaining sufficient breakdown voltage to sustain operation* is the InP HBT system, with SHBTs represented by the blue line, PHBTs by the red line, type-I DHBTs by the green line, and type-II GaAsSb DHBTs by the orange line. Noted in the figure is the 1.3V breakdown advantage the InP/GaAsSb DHBT system offers over the InP/InGaAs SHBT system. InP pseudomorphic high-electron mobility transistors (pHEMTs, purple) currently demonstrate extremely high speeds, reaching f_T values of 562 GHz. In order to achieve these speeds, however, the pHEMT transistor must be biased precariously close to the breakdown (0.85 V), which suggests the limit to scaling these devices has been reached.

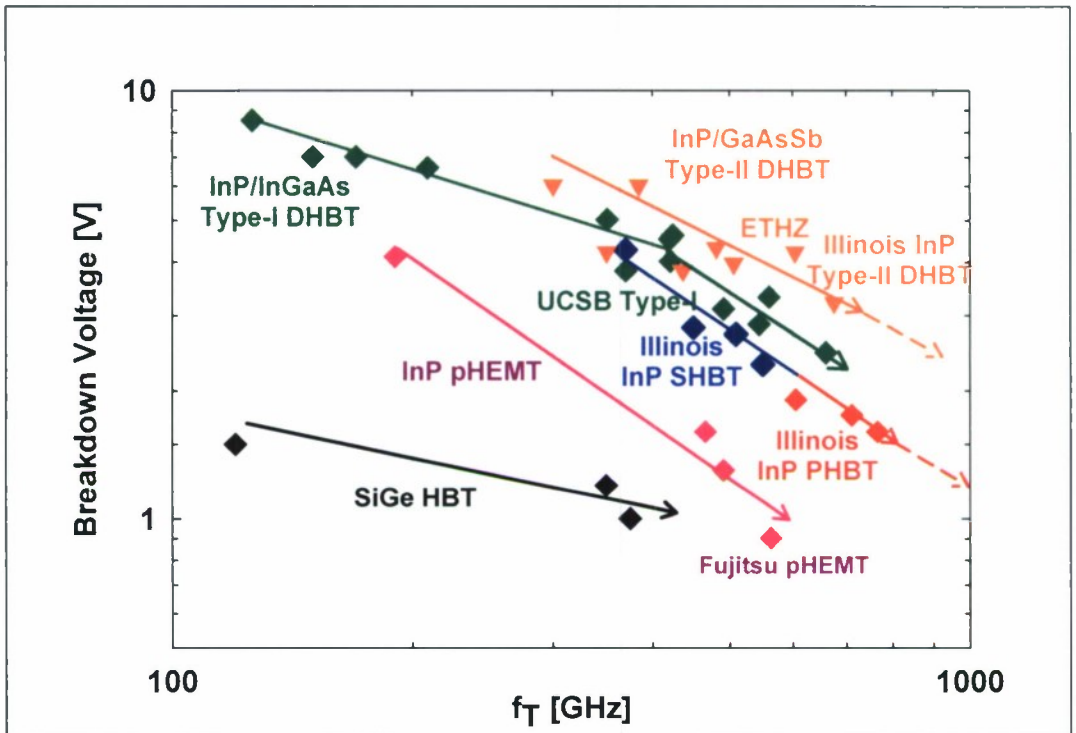
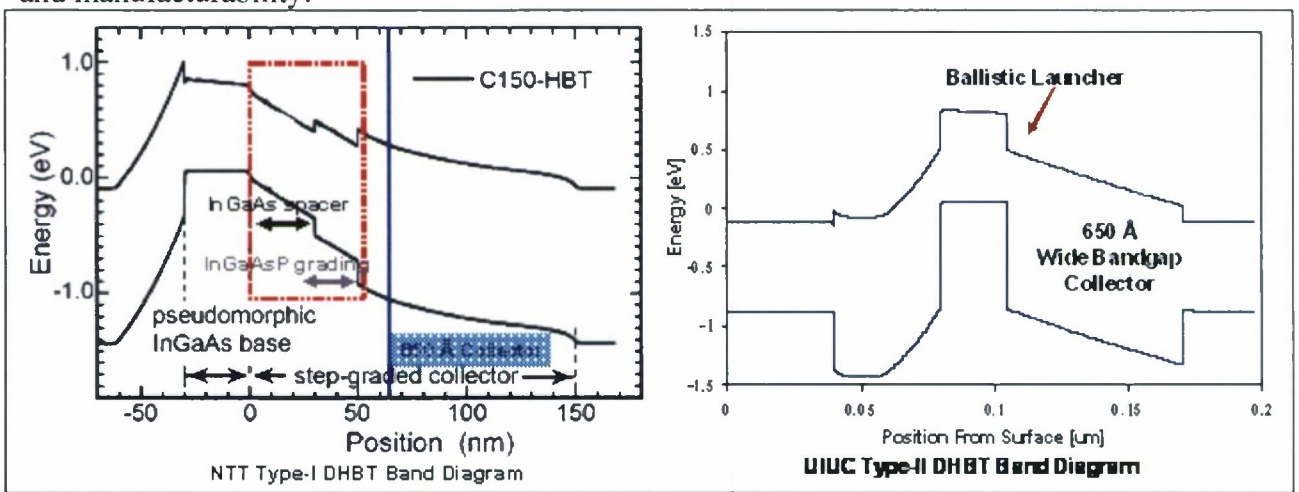


Figure A-1: f_T versus breakdown voltage for various material systems, taken from M. Feng, S.C. Shen, D. Caruth, and J-J Huang, invited paper, in Proc. IEEE, Vol. 92, no.2, pp. 354-375, Feb. 2004

It is important to note that the InP/InGaAs DHBT material system (green in Figure A-1) is exhibiting sharp drop-offs in breakdown voltage as the collector is thinned (dashed green line in Figure A-1). This behavior, although undesirable, is inevitable due to the collector being primarily composed of InGaAs/InGaAsP spacer layers rather than wide bandgap InP as illustrated by Figure A-2. On the hand, the type II DHBT did not require any transition or graded region, hence, it is a fundamental better device choice for both higher speed operation and manufacturability.



(a) (b)

Figure A-2: (a) Type-I DHBT energy band diagram illustrating grading schemes required to eliminate current blocking discontinuity at base-collector junction. (b) UIUC Type-II DHBT band diagram illustrating energetically favorable discontinuity of Type-II alignment.

As shown in Figure A-3, the breakdown voltages of type-I DHBTs converge to those of SHBTs as the collectors are thinned to achieve higher speeds, while the type-II devices are able to maintain a more favorable trend. InP/GaAsSb type-II DHBTs do not exhibit the degradation in breakdown voltage or limitation in achievable current density experienced in type-I DHBTs, having demonstrated the high-speed operation (f_T > 500 GHz), current densities of 15 mA/μm^2 and breakdown voltages above 4 V for millimeter-wave power applications.

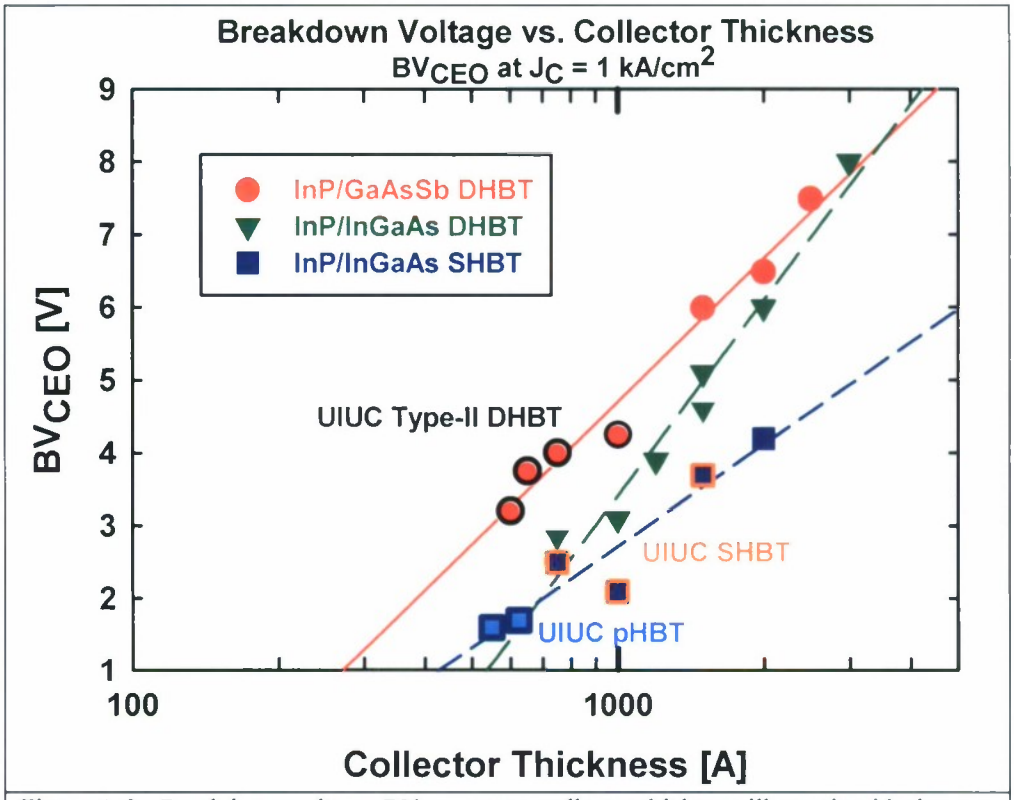


Figure A-3: Breakdown voltage, BV_{CEO}, versus collector thickness illustrating ideal scaling of GaAsSb DHBTs (red line), and degradation of the breakdown of type-I DHBTs for scaled collector thicknesses (green line), after H. G. Liu, S. P. Watkins, and C. R. Bolognesi, IEEE TED, vol. 53, 2006.

As briefly mention earlier, the base-collector junction of type-II DHBTs intrinsically provides a beneficial energy line up in the conduction band that serves to launch electrons into the collector with a significant amount of initial energy (Figure A-4(a)). This initial energy serves to increase the velocity at which the electrons enter the depleted collector, giving reduced collector transit times, if this initial velocity can be maintained or increased throughout the entire collector. Over short distance, distances on scale with the thickness of UIUC's 1000Å collectors, electrons can be injected with energies greater than the InP L-valley energies without a significant number of carriers scattering to this low mobility valley (Figure A-4(b)).

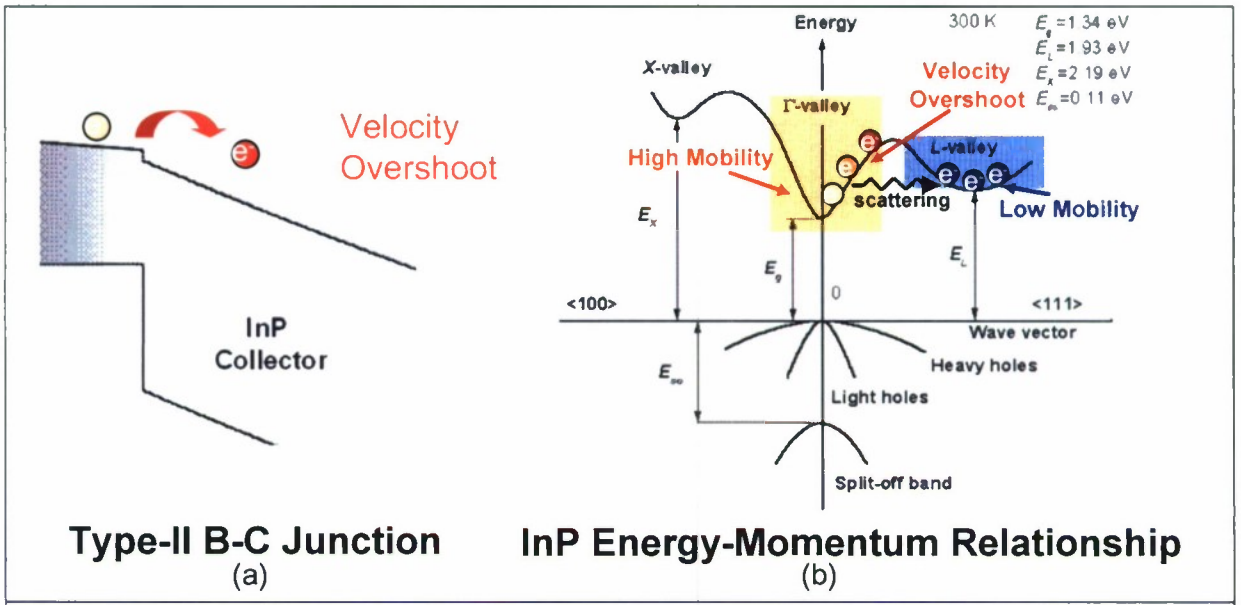


Figure A-4: (a) Type-II base-collector band offset showing energetic injection of carriers into the collector. (b) InP energy-momentum relationship showing the possibility of intervalley scattering from the Γ-valley to the L-valley. Over short distance little scattering occurs allowing high carrier velocities throughout the entire collector.

This lack of significant scattering results in an average carrier velocity that is much greater than the maximum electron velocity in bulk InP. Average collector velocities have been extracted from measured data, as can be seen in Figure A-5, and have been found to be upwards of 4E7 cm/s, greater than 1.5 times the bulk InP saturation velocity. These increased carrier velocities greatly reduce the collector transient time (τ_C) of these type-II DHBTs, giving them a significantly smaller τ_C than type-I DHBTs with an identical collector thickness. As can be seen in Figure A-6, this reduction in collector transient time serves to increase the unity current gain frequency of a device. This increased carrier velocity, through energetic carrier injection and velocity overshoot throughout the collector, also allows for the use of thicker collectors with a smaller speed penalty than that which is present in a type-I device. Since for a given f_T/f_{MAX}, type-II DHBTs can have a thicker collector than type-I DHBTs and type-II wide-gap collectors are less prone to breakdown, the type-II device will have a much higher breakdown voltage, making it the clear choice for high power millimeter wave DHBT amplifiers.

	G9478 Uniform 250/600Å	G9486 Graded 250/600Å	G9500 Graded 300/600Å	G9520 Graded 200/600Å	G9537 Graded 300/1000Å
τ_B [fs]	157	81	111	66	111
τ_C [fs]	104	105	81	81	125
v_{eff} [10^7 cm/s]	3.13	3.09	3.72	3.72	4.01

D_n = 29.6 cm²/s ΔE = 0.053 eV v_{sat} = 4.85 x 10^7 cm/s

Figure A-5: Measured base and collector transient times and extracted effective collector velocity for different base and collector structures.

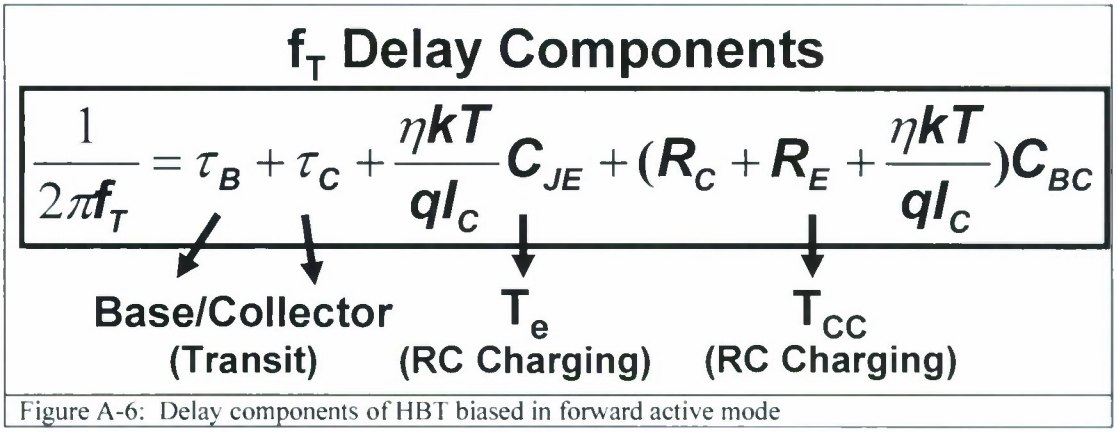


Figure A-6: Delay components of HBT biased in forward active mode

Utilizing vertical device scaling and compositional base grading, a 0.37 x 7.6 um^2 type-II DHBT with a 20 nm base and 60 nm collector was fabricated with a peak f_T and simultaneous f_{MAX} of 690GHz/185GHz at a temperature of 25 °C and an f_T/f_{MAX} of 745GHz/205GHz at a temperature of -37 °C (W. Snodgrass, et al. IEDM 2007). Measured and extrapolated values of h_{21} and the unilateral power gain are shown in Figure A-7 for both temperatures. Peak f_T occurred at a current density of 12.8 mA/um^2 with a collector base voltage of 0.15 V.

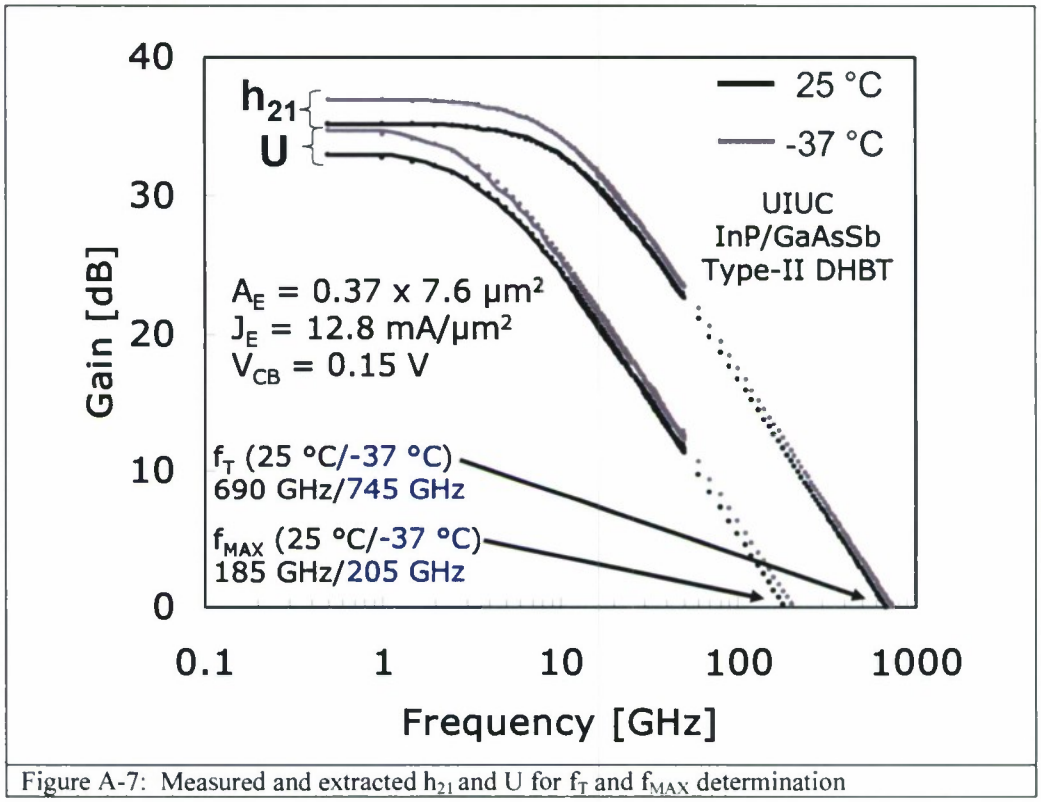


Figure A-7: Measured and extracted h_{21} and U for f_T and f_{MAX} determination

DC characteristics of a similar device are shown in Figure A-8. The device has a DC current gain of 82 and a BV_{CEO} of 3.2V. Here the breakdown voltage is defined for a current of 1 kA/cm^2.

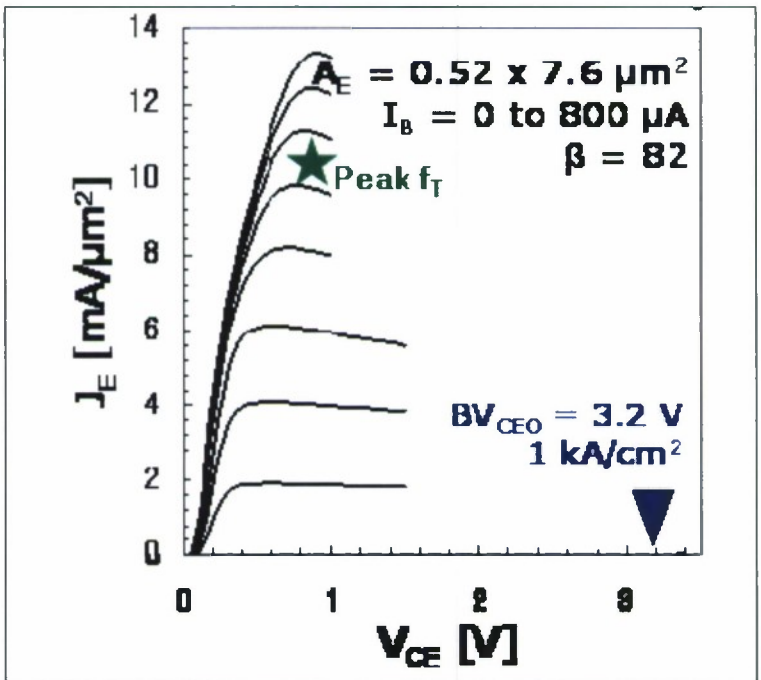


Figure A-8: Measured DC characteristics and breakdown

Vertical scaling tends to drastically increase the f_T of a device while significantly reducing the simultaneous f_{MAX}. This can be understood through the relationship between the f_T and f_{MAX} of an HBT device shown in Figure A-9. As the device shrinks vertically, the thickness of the base and collector materials shrinks. Shrinking the base increases the base resistance and shrinking the collector increases the base-collector capacitance, both of which are detrimental to the f_{MAX} of the device. By increasing the thickness of the base and collector layers it is possible to essentially trade f_T performance for f_{MAX} performance. Increasing the layer thickness, while increasing the overall carrier transit time and lowering f_T, reduces the parasitics associated with the device and increases its maximum power gain frequency.

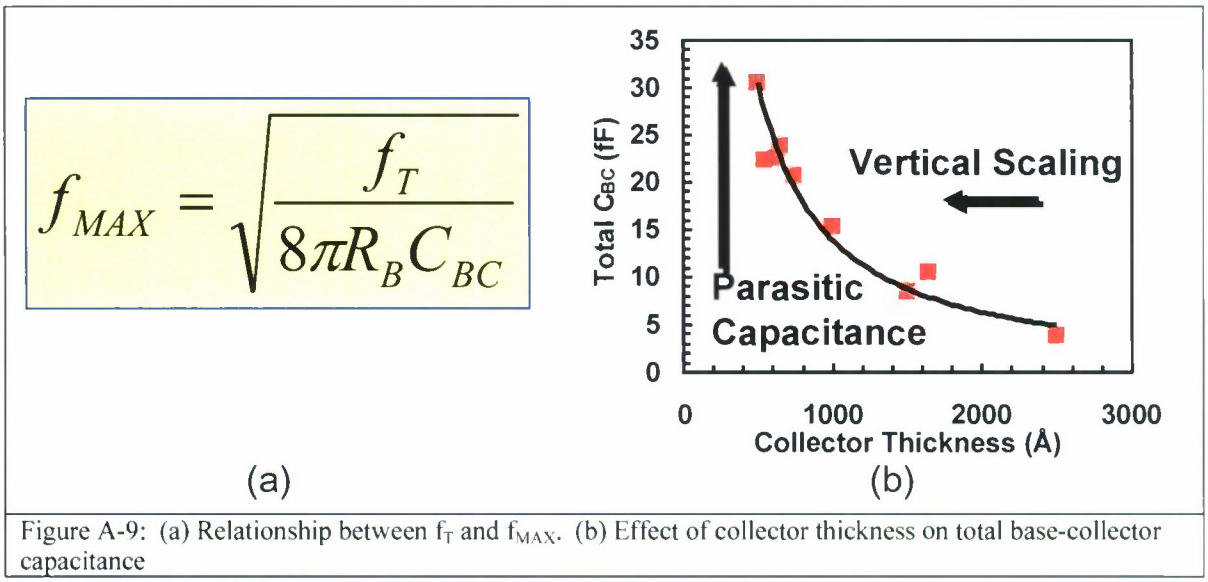


Figure A-9: (a) Relationship between f_T and f_{MAX}. (b) Effect of collector thickness on total base-collector capacitance

In an attempt to trade off f_T for f_{MAX}, thicker devices with a 30 nm base and 100 nm collector were fabricated. Peak f_T/f_{MAX} performance of 480 GHz/420 GHz was seen for 0.46 x 3.1 um^2 devices at a temperature of 25 ^oC. Peak performance occurs at a current density of 7.6 mA/um^2 at a base-collector potential of 0.4 V. The f_T and f_{MAX} extrapolation are detailed in figure A-10.

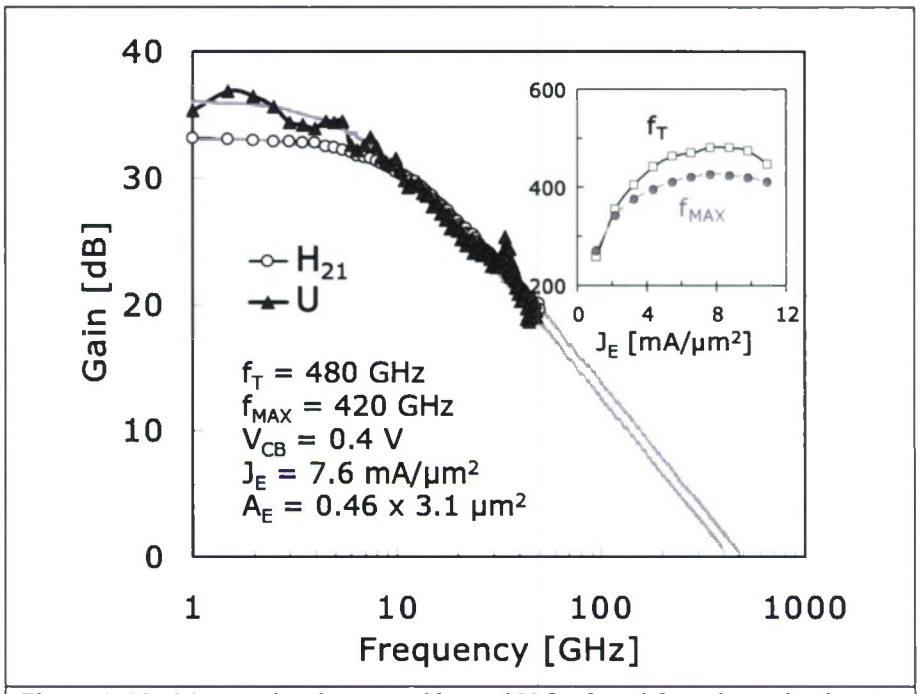


Figure A-10: Measured and extracted h_{21} and U for f_T and f_{MAX} determination

The breakdown voltage of this device is increased to 4.3 V, as would be expected with a thicker 1000 Å collector. The thicker base gives a lower DC current gain (β). Figure A-11 shows a full DC family of curves.

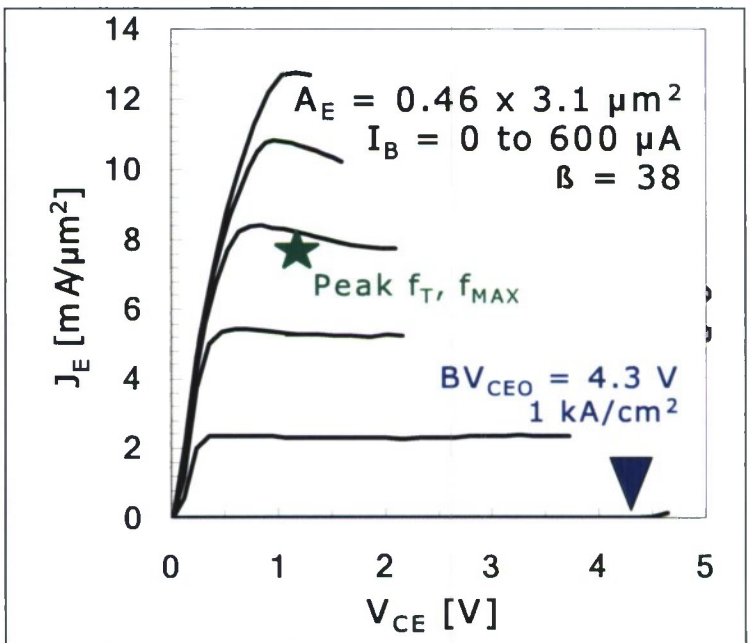


Figure A-11: Measured DC characteristics and breakdown

UIUC has a clear two part plan which it is using to develop a device that will achieve an f_T/f_{MAX} of 400/650 GHz with a $BV_{CEO} > 5V$. UIUC is using higher quality, commercially grown material and refining the fabrication process for 180 nm wide emitters. Through the use of commercially grown wafers, the base sheet resistance can be reduced by a factor of 2 to 3 from wafers grown in house, thereby reducing the overall base resistance and increasing the f_{MAX} of the device. Wafers grown at UIUC have a typical base sheet resistance of 2000 ohm/sq. for a uniform base layer and sheet resistances of 2800 ohm/square for graded base layers, whereas commercially grown uniform bases have sheet resistances around 900 ohms/square and graded layer sheet resistances of 1200 ohms/square. Measured results showing sheet resistance versus base thickness for multiple UIUC and commercially grown wafers is shown in Figure A-12(a). In addition to improved sheet resistance, commercially grown wafers have also been shown to have much lower contact resistance as is shown in Figure A-12(b).

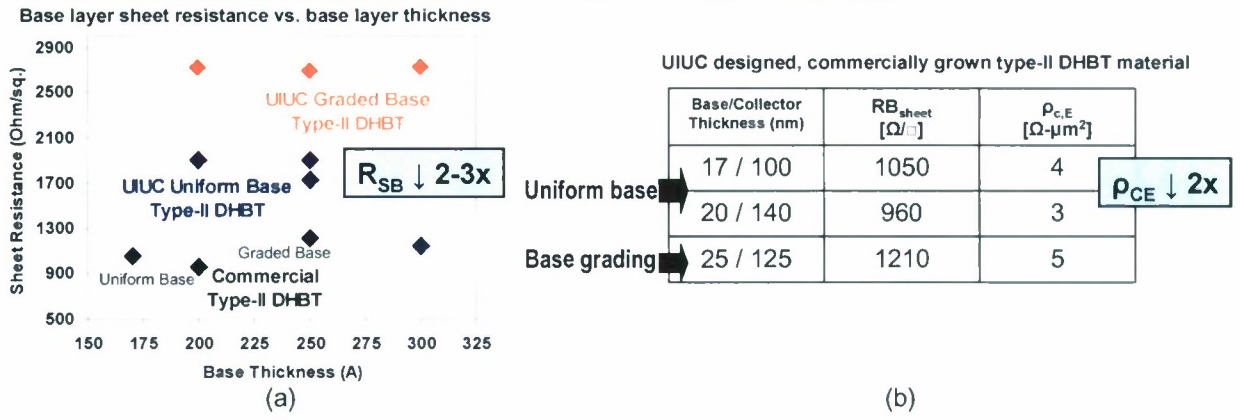


Figure A-12: (a) Comparison of the base sheet resistance of commercially grown wafers to wafers grown at UIUC. (b) Measured base sheet resistance and emitter contact resistance of UIUC design, commercially grown type-II DHBT material.

In addition to using commercially grown material, UIUC is developing its high speed device process for the fabrication of DHBTs with 180 nm wide emitters in order to reduce the intrinsic base-emitter capacitance. Reduction of the emitter capacitance serves to increase both f_T and f_{MAX}. Projections, shown in Figure A-13 below, using the measured properties of two new commercially grown strained GaAsSb wafers combined with a 180 nm fabrication process show that a 400/650 GHz f_T/f_{MAX} device with a breakdown voltage of 5 V can be achieved for a device with a 20 nm base and 140 nm collector. Due to the low base sheet resistivity of the commercially grown base layer, the base can be kept thin to increase f_T while not significantly affecting f_{MAX} performance. A thick 140 nm collector gives the reduction in base-collector capacitance and effectively trades current gain for power gain while increasing the breakdown voltage of the device. As the 180 nm device process has not yet been perfected, no full devices have been completely fabricated on these commercially grown wafers.

Emitter			**Emitter**		
width	**180**	nm	width	**180**	nm
contact resistivity	3	$\Omega\cdot\mu m^2$	contact resistivity	3	$\Omega\cdot\mu m^2$
Base			**Base**		
thickness	17	nm	thickness	20	nm
contact width	**100**	nm	contact width	**100**	nm
contact resistivity	8	$\Omega\cdot\mu m^2$	contact resistivity	8	$\Omega\cdot\mu m^2$
sheet resistance	1200	$\Omega/\square$	sheet resistance	1000	$\Omega/\square$
Collector			**Collector**		
thickness	100	nm	thickness	140	nm
current density	8	$mA/\mu m^2$	current density	6	$mA/\mu m^2$
BV_{CEO}	4	V	BV_{CEO}	**>5**	V
	f_τ **470** GHz			f_τ **400** GHz	
	f_{max} **550** GHz			f_{max} **650** GHz	

Figure. A-13: Projections for two of the new strained GaAsSb base commercial wafers combined with 180 nm fabrication process

Task S2(b): Develop large signal DHBT model (SDD2-POWER) to enable power amplifier design.

In this program the UIUC SDD model was further developed to specifically model type-II DHBT devices operating with large signal swings such as in power amplifier circuits. The UIUC SDD model has been in development for over 10 years. Development of this model was initiated due to the VBIC (Vertical Bipolar Inter-Company), the leading compact bipolar model of the time and current industry standard, model's fundamental inability to properly model HBT devices. The VBIC model was developed for implanted silicon homojunction bipolar transistors, not epitaxially grown HBT devices, and therefore cannot accurately model many of the characteristics of modern HBTs. Since the VBIC model is tailored for silicon devices, it cannot model heterojunction effects such as current blocking or velocity modulation at or in the collector. Figure B-1 shows a schematic of the VBIC model. It is easy to tell that this model was developed for an implanted device from the parasitic pnp-transistor modeling found between the base, substrate, and collector.

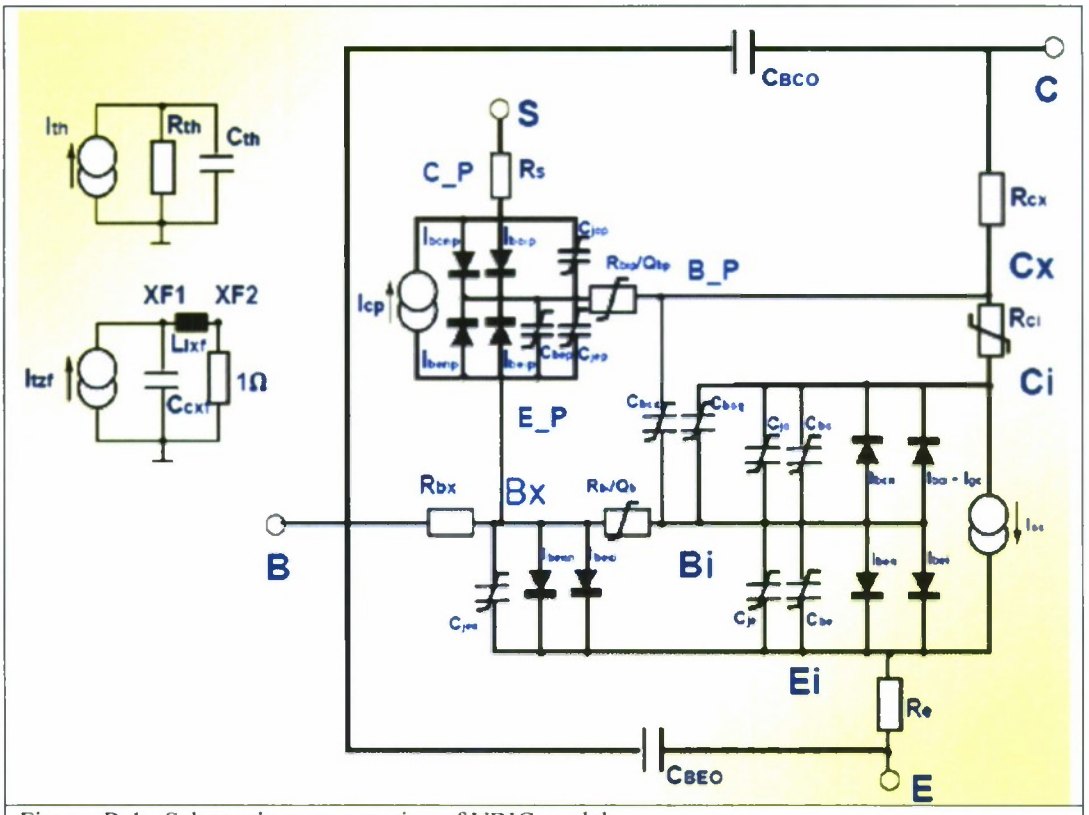


Figure. B-1: Schematic representation of VBIC model

A SDD model development timeline and symbolic model schematic are shown in figure B-2. The UIUC SDD model initially started as a SHBT model based around the well known Gummel-Poon integral charge control relationship. With the addition of Kirk effect modeling, self-heating, and passive parasitics, it was found to be capable of accurately modeling SHBT devices. In order to accurately model type-I DHBT devices, the effects of the base-collector heterojunction interface had to be added to the model. Updating the SHBT model to a type-I DHBT model entailed adding equations to account for the heterointerface current blocking that occurs at the BC junction due to the positive energy barrier seen by electrons transitioning between the base and collector layer at low voltages and high currents. This current blocking manifests itself as a rounded 'knee' on the I-V family of curves plot. In addition to the accurate modeling of the current blocking, equations were added to the model that modeled the change in collector transient time across applied current and voltage, an important parameter for the modeling of f_T. Later type-I SDD2 model development added realistic device scaling and rudimentary noise modeling to the model.

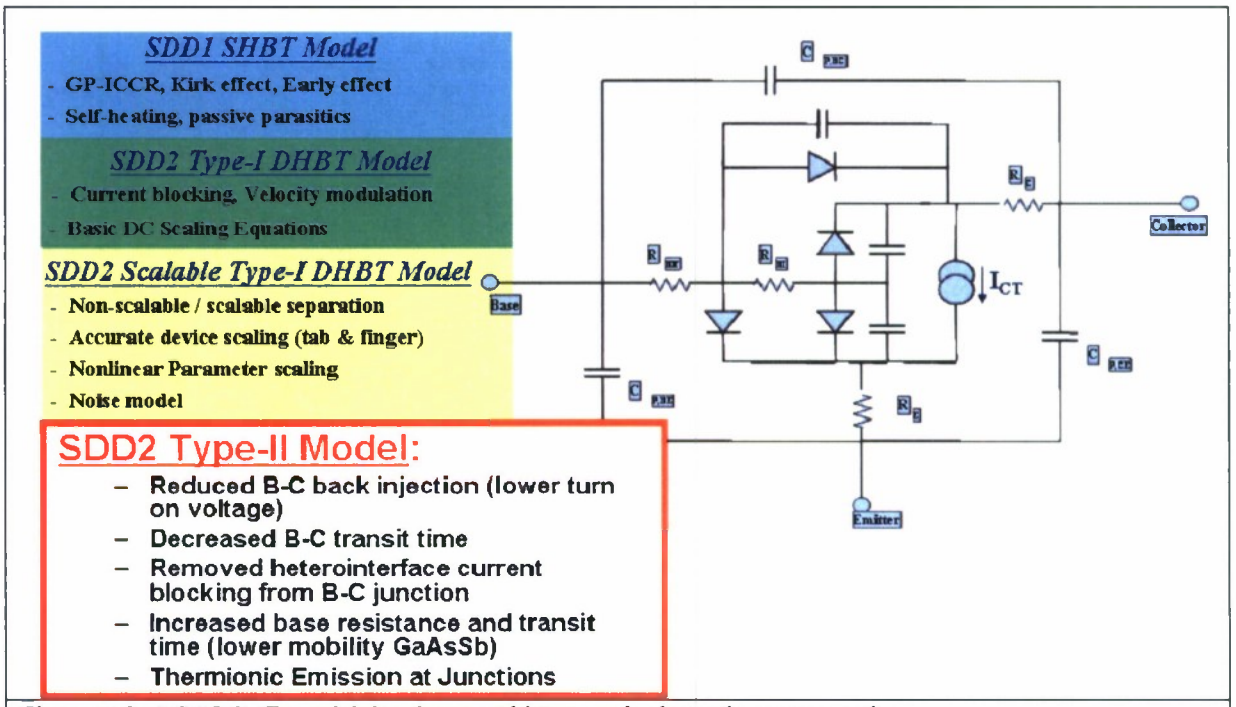


Figure B-2: UIUC SDD model development history and schematic representation.

The type-I UIUC SDD model, because it was specifically developed to model HBTs, has been shown to be much more accurate in modeling DHBTs than the industry standard VBIC model. Figure B-3(a) shows a comparison between the measured characteristics of a 0.5 x 5.2 um^2 device fabricated at Vitesse Semiconductor and those characteristics predicted by the VBIC model extracted and distributed by Vitesse. Figure B-3 (b) shows a comparison between the same device and the type-I UIUC SDD2 model. It is clearly obvious that the SDD2 model more accurately models all aspects of the device such as current gain, turn on voltage, knee current rounding due to current blocking, high current self-heating, etc. In this work, the modeling ability of the type-I SDD2 model was extended to be capable of accurately modeling the high frequency type-II power devices fabricated by UIUC.

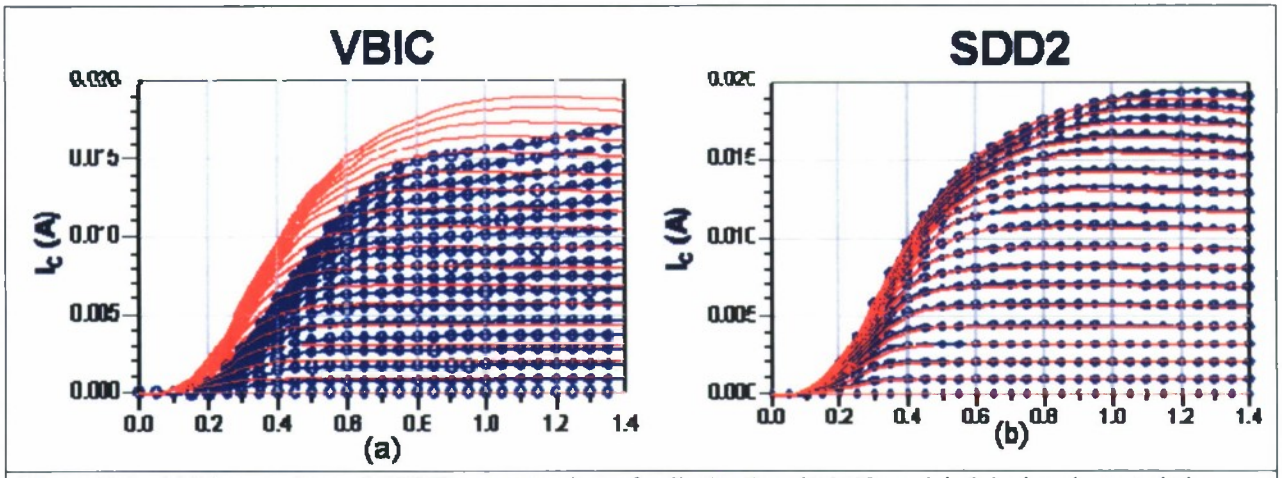


Figure B-3: (a) Measured type-I DHBT current-voltage family (red) and VBIC modeled device characteristics (**blue**). (b) Measured type-I DHBT current-voltage family (red) and SDD2 modeled device characteristics (**blue**).

Changes were required to update the type-I SDD2 model into a model that could correctly model the physics of type-II devices. A comparison of the band structures of type-I and type-II devices is shown in figure A-2 in the previous section. The prime difference between these structures is the location of the base conduction band relative to the conduction band of the emitter and collector at equilibrium. In type-II devices, carriers are no longer energetically injected into the base, but are injected with energy into the collector, increasing the base transit time and reducing the collector transit time. Also since the collector conduction band is inherently lower than the base, it is harder for electrons to be injected from the collector into the base. This is modeled by reducing the magnitude of current injected from the collector to the base, and essentially results in lowering the Vce turn on voltage. The base resistance is increased to properly model the increased sheet resistance of GaAsSb over InGaAs. The amount of current blocking modeled is also reduced to account for the lack of a positive energy barrier at the collector.

Effort was focused on extracting the new type-II SDD2-POWER model for the 480/420 GHz type-II device fabricated at UIUC and described in Section A. Measured and modeled DC I-V and V-V curves can be seen in figure B-4. Accurate fits are achieved for both curves.

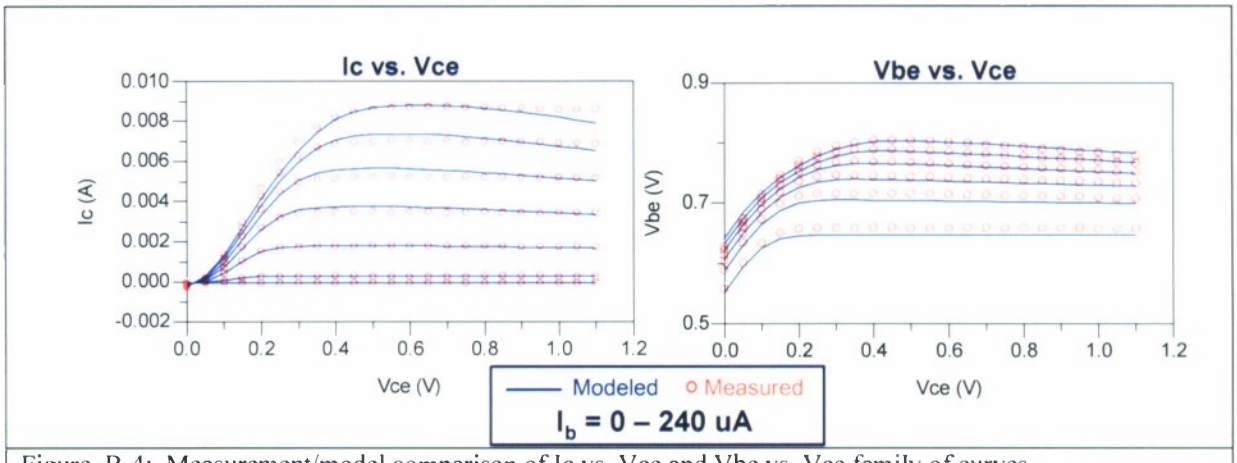


Figure. B-4: Measurement/model comparison of Ic vs. Vce and Vbe vs. Vce family of curves

Figure B-5 shows a comparison between measured and modeled RF data. The accurate modeling of the type-II transit and charging times give a good fT fit to the measured device data. The device's fMAX performance is slightly under-predicted.

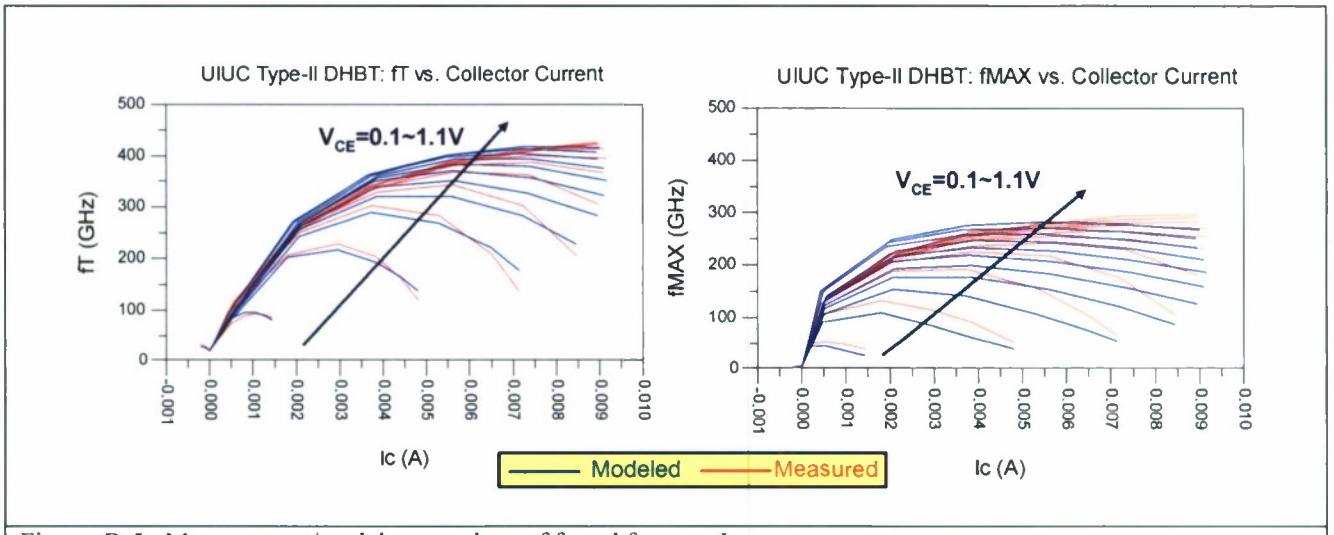


Figure. B-5: Measurement/model comparison of f_T and f_{MAX} vs. Ic

In order to assess the new UIUC SDD2-POWER model's ability to correctly model device performance under larger signal swings, single tone measurements were taken and compared to modeled results. A diagram of the single tone measurement is shown in figure B-6. Essentially a single tone at a given frequency and power is input into the device and the multiple output tones that are generated by the nonlinear device are measured. This measurement was taken on a 0.3 x 8 um^2 device, and the first three output harmonics were measured.

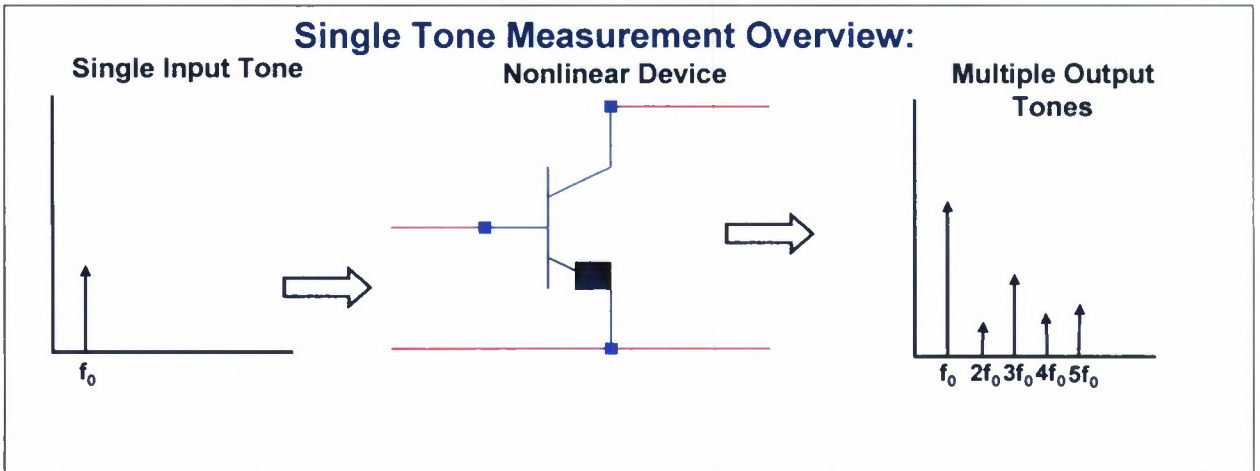


Figure. B-6: Single tone measurement overview

The new model is shown to be accurate in its prediction of output harmonics at both high and low biases. Figure B-7 shows the measured and modeled magnitude of the third order harmonic taken at high and low biases as the power of the input tone is swept. The type-II SDD2 model accurately predicts the power level and compression that occurs at the output harmonic as the input power is swept. It is the third harmonic that is primarily responsible for gain

compression at high powers, making this kind of modeling accuracy is crucial for the accurate design and simulation of high frequency power amplifiers.

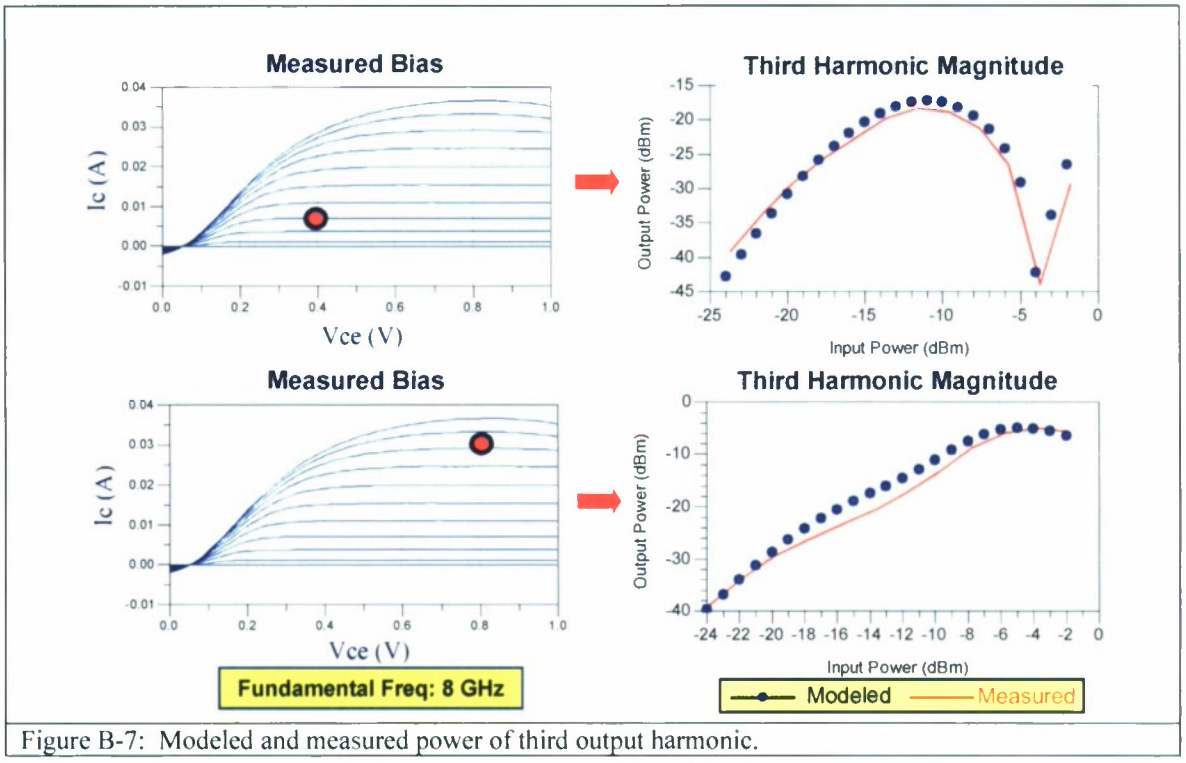


Figure B-7: Modeled and measured power of third output harmonic.

Task S2(c): Design/Simulation of 340 GHz MMIC power amplifier with gain > 10 dB and Pout > 10 mW

The parameters of the type-II SDD2 model of the 480/420 GHz f_T/f_{MAX} device were updated to simulate a 480/600 GHz device. With this model a 340 GHz power amplifier having a gain of 10 dB and an output power greater than 10 mW is designed. The primary updates to the model were the reduction of the base resistance to reflect the improved sheet resistance of the commercially grown material and the slight reduction the base-collector capacitance resulting from a slightly thicker collector. The plots of H21 and U vs. frequency are shown in Figure C-1. To achieve this RF performance the model was biased at a Vce of 1.1V and an Ib of 120 uA. This modeled device draws 7.86 mA of current for a power consumption of 8.62 mW per device.

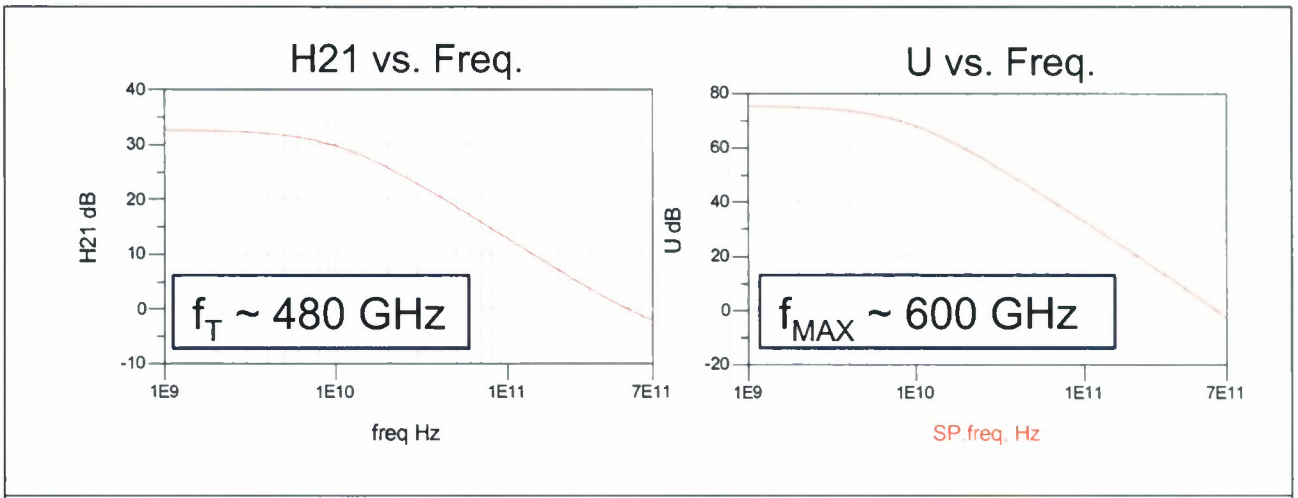


Figure. C-1: Modeled h_{21} and U of a hypothetical device fabricated using commercially grown material and a 140 nm collector.

From harmonic balance simulations, it was found that the maximum output power for which a three stage amplifier can achieve a gain of 10 dB is approximately 5.4 dBm. So in order to achieve the required 10 mW output power, three identical three stage amplifiers need to be power combined. A block diagram of the overall power amplifier is shown in Figure C-2.

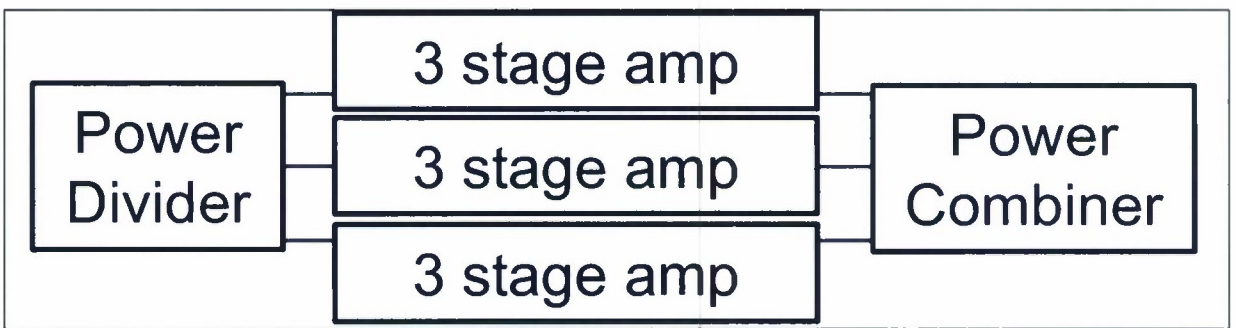


Figure C-2: Block diagram of power amplifier design.

Each amplifier chain consists of 3 cascaded conjugately matched transistors. Bias voltages are provided through matching stubs, and each stage is capacitively coupled to the next stage. A schematic of the three amplifier stages is shown in Figure C-3.

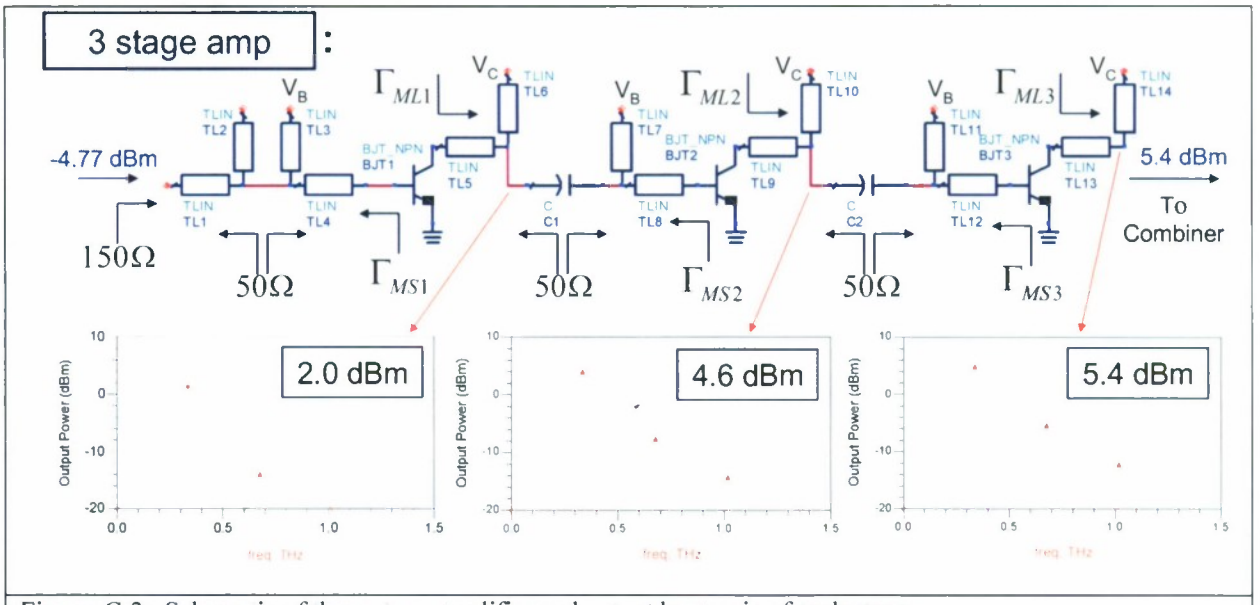


Figure. C-3: Schematic of three stage amplifier and output harmonic of each stage

From figure C-3 it is evident that as the magnitude of the signal increases, the gain of each amplifier becomes significantly compressed and the output signal becomes more distorted. The gain of the last stage is actually less than 1 dB. In this modeled circuit, all passive components have been considered to be ideal. The overall circuit has a DC power draw of 77.6 mw and a linear power gain of 9.47 mW, giving it a power added efficiency of 12.2%. This of course would be lower if transmission line loss were taken into account.

Conclusion:

In summation, UIUC successfully fabricated a world record type-II device with f_T/f_{MAX} of 690/185 GHz having a breakdown voltage of 3.2V (W. Snodgrass, et al. IEDM 2007), and a device for which f_T was traded off for increased f_{MAX} of 480/420 GHz (f_T/f_{MAX}) with an increased breakdown voltage of 4.3V. Updates were made to UIUC's type-I SDD2 model, which has been proven to be superior to the industry standard VBIC model in modeling type-I DHBT operation, to model type-II device operation. This type-II SDD2 model was then used to model the fabricated 480/420 GHz device. Parameters of this model were shifted to approximately reflect the new material and fabrication techniques, which resulted in a modeled 480/600 GHz device. This projected model is then used to design a 340 GHz MMIC power amplifier with a gain greater than 10 dB and an output power of more than 10 mW.

UIUC has a clear plan for the development of a 400/650 GHz f_T/f_{MAX} device. It will entail the use of commercially grown material and an updated fabrication process. Material from the commercial vendor has already been received. Once the fabrication process is successfully updated, UIUC is confident that we can produce devices that meet our projections of an f_{MAX}>650 GHz.

Bibliography:

[1] W. Snodgrass, B.-R. Wu, K. Y. Cheng, and M. Feng, "Type-II GaAsSb/InP DHBTs with Record fT = 670 GHz and Simultaneous fT, fMAX > 400 GHz," presented at International Electron Devices Meeting, Washington D.C., 2007.

[2] H. G. Liu, S. P. Watkins, and C. R. Bolognesi, "15-nm base type-II InP/GaAsSb/InP with F_T=384 GHz and a 6-V BV_{CEO}," IEEE TED, vol. 53, 2006.

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13. ABSTRACT (Maximum 200 words)

The proposed program goals are the development of transistor technology for the sub-millimeter wave (i.e 340GHz) source to be used in a wide range of military and consumer applications using transistors operating toward THz bandwidths. The transistors will be designed, developed and fabricated using a novel material structure employing a type II double heterojunction bipolar transistor (type II DHBT). This structure has a world-record high-speed operation (ft >500 GHz) with higher breakdown voltage and lower junction temperatures than any other competing technology, including lattice matched type I InP/InGaAs I SHBTs, type I DHBTs, and pseudomorphic high-electron mobility transistors (pHEMTs).

We propose to accomplish these using Antimonide-based DHBTs for all active components of the power amplifier. This project will be broken up into three stages consisting of a transistor development and fabrication stage, a model development stage, and a power amplifier design stage. In the transistor development and fabrication stage the speed of Sb-DHBTs will be increased to reach the goal of 650/400 GHz (fMAX/fT). Device models (Agilent ADS and UIUC's own SDD2) will be refined to accurately represent the devices high frequency characteristics and enable the design of the power amplifier's components. Finally a power amplifier operating at 340GHz will be designed and simulated to assess power gain, maximum output power, and power added efficiency.

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(a) Papers published in peer-reviewed journals (0)
(b) Papers published in non-peer-reviewed journals (0)
(c) Presentations
  i. Presentations at meetings, but not published in Conference Proceedings (0)
  ii. Non-Peer-Reviewed Conference Proceeding publications (0)
  iii. Peer-Reviewed Conference Proceeding publications (1)

2007 IEDM: *"Type-II GaAsSb/InP DHBTs with Record fT = 670 GHz and Simultaneous fT, fMAX > 400 GHz"*

2007 Mantech: *"The Development of a Symbolically Defined Large Signal InP/GaAsSb Type-II DHBT Model for 200 GHz Mixed Signal Circuit Simulation"*

(d) Manuscripts (0)
(e) Books (0)
(f) Honors and Awards (0) – Stillman Award (Snodgrass)
(g) Title of Patents Disclosed during the reporting period (0)
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(a) Graduate Students: William Snodgrass and Mark Stuenkel
(b) Post Doctorates: None
(c) Faculty: Milton Feng, (1 month)
(d) Undergraduate Students: None
(e) Graduating Undergraduates: None
(f) Masters Degrees Awarded: None
(g) Ph.D.s Awarded: None
(h) Other Research Staff: None

(3) – Technology Transfer: Technology discussion with Agilant (Santa Rosa)

(4) – Scientific Progress and Accomplishments

- UIUC successfully fabricated a world record speed type-II InP DHBT with f_T/f_{MAX} of 690/185 GHz having a breakdown voltage of 3.2V (W. Snodgrass, et al. IEDM 2007),
- UIUC made type II DHBT for which f_T was traded off for increased f_{MAX} of 480/420 GHz (f_T/f_{MAX}) with an increased breakdown voltage of 4.3V.

(5) – Copies of technical reports: None